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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/037,671	01/03/2002	Norm Hendrickson	47225/DMC/V165	8282

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EXAMINER
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WONG, LINDA

ART UNIT	PAPER NUMBER
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2634

DATE MAILED: 03/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

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<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/037,671	HENDRICKSON, NORM	
	<b>Examiner</b>	<b>Art Unit</b>	
	Linda Wong	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 03 January 2002.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-21 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-7, 9, 10, 13, 14 and 18-21 is/are rejected.
- 7) ☒ Claim(s) 8, 11, 12 and 15-17 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 03 January 2002 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                        | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)               | Paper No(s)/Mail Date. _____  |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____  | 6) <input type="checkbox"/> Other: _____                                    |

## **DETAILED ACTION**

### ***Drawings***

1. The drawings are objected to because Figures 1 and 3 need arrows indicating the direction of the output(s) and input(s) to the components for better clarification.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

### ***Specification***

2. The disclosure is objected to because of the following informalities:
  - a. On page 1, paragraph [0013], line 7,8, and 12, the term "N" should be defined. Also, on line 8, the term "n" should be changed to "N" if "n" is same reference as "N" described in the paragraph. This will keep consistency and clarity when referring to this term.
  - b. On page 1, paragraph [0014], line 2, the term "reference clock" is recited in this paragraph and in claim 1. If this term is equivalent to the reference clock recited in claim 1, the term needs to be defined. For example, is the reference clock mentioned equivalent to "the external clock signal"?

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- c. In Fig. 3, the labels 139a – d and D0+/- to D15+/- are not disclosed in the specification.
- d. On page 3, paragraph [0029], line 2, the delay line mentioned is labeled as 37. In Fig. 3, the delay line is labeled as 137. It is suggested that the label is changed to 137 in the specification to match the diagram.

Appropriate correction is required.

### ***Claim Objections***

- 3. **Claim 18** is objected to because of the following informalities:
  - a. **Claim 18**, line 5 and 6, recite terms “N” and “K”. These terms should be defined within the claim. Appropriate correction is required.

### ***Claim Rejections - 35 USC § 112***

- A. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

- 4. **Claim 1** are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

- a. **Claim 1** recites a second counter "receiving the control signals and the selected clock signal" and a first counter "receiving the control signals and selecting a clock signal and adjusting the output signal" and a first phase detector "comparing a data signal to an output signal". Based on the recitation, the first phase detector is connected to the first counter. In the specification and drawings, the first counter receives 3 inputs: two control signals and the output from another counter (the selected clock signal).

B. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. **Claim 1** recites "control signals" generating by both the first and second phase detector. To clarify which control signals are being processed by the first and second counter, it is suggested that a term, such as "first" and "second", be placed before the appropriate control signals.
6. **Claim 1** recites "the selected clock signal" generated by the first counter. To clarify the selected clock signal produced by the first counter is received by the second counter, it is suggested that a term, such as "first", be placed before the selected clock signal.

***Claim Rejections - 35 USC § 102***

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. **Claims 1, 2, 3, 5, 6, 7, 8, 9, 10, 13, 21** are rejected under 35 U.S.C. 102(b) as being unpatentable by Ozkan (US Patent No.: 5488641) in view of Fawcett et al. (US Patent No.: 6320436).
- a. **Claim 1**, Ozkan discloses a phase detector (Fig. 2, label 240) comparing a data signal (Fig. 2, label input data signal) to an output signal (Fig. 2, recovered clock signal) and outputs control signals (Fig. 2, outputs from 240), a counter (Fig. 2, label 230) selecting an offset clock signal (Fig. 2, output to mux 220) based on received control signals (Fig. 2, output from 230 to mux 220) and output from the counter (Fig. 2, label 290), which is used to select a clock signal (Fig. 2, output from 290 to mux 280) and adjust the output signal (Fig. 2, recovered clock signal) corresponding to the selected clock signal (Fig. 2, output from 230 to mux 220), a phase detector (Fig. 2, label 270) comparing a reference clock signal (Fig. 2, label 200) with a delayed clock signal (Fig. 2, output from label 280 to 270) and generating control signals (Fig. 2, output from label 270), and a counter receiving control signals (Fig. 2, output from label 270 to 290) and selecting an offset clock signal (Fig. 2, output from label 290 to 280).
- b. **Claim 2**, Ozkan discloses a multiplexor (Fig. 2, label 220) generating the output signal based on the output from counter (Fig. 2, label 230).
- c. **Claim 3**, Ozkan discloses a second multiplexor generating the offset clock signal (Fig. 2, label 280) based on the selection from a counter).

- d. **Claim 5**, Ozkan discloses a delayed signal (Fig. 2, output from mux 280) dependent on an offset clock signal. (Fig. 2, output from mux 220 and 210)
- e. **Claim 6**, Ozkan discloses delayed clock signal (Fig. 2, output from the mux 280) offset by the selected clock signal (Fig. 2, output from mux 220). Although Ozkan does not disclose that the delay line, wherein the delayed clock signal is half a clock period of the offset clock signal, Fawcett et al discloses a delay line "delayed by a selected amount." It would be obvious to one skilled in the art to delay the taps disclosed by Ozkan by any selected amount based on design choice.
- f. **Claim 7**, Ozkan discloses a method of generating a plurality of clock signals based on a reference clock signal (Fig. 2, labels 200, and outputs from 210), selecting one of the plurality of clock signals based on a phase signal (Fig. 2, label recovered clock signal, and output from 230), generating the phase signal based on a plurality of clock signals and data signals (Fig. 2, label 200, output from mux 280, input data signal and recovered clock signal), generating a reference signal based on a reference clock signal and delayed clock signal (Fig. 2, label 200, output from mux 280 and output from counter 290 to mux 280), and adjusting the selected one of the plurality of clock signals based on the generated reference signal (Fig. 2, label recovered clock signal, output from mux 280 to mux 220).
- g. **Claim 9**, Ozkan discloses a delay line delaying the reference clock signal, which would approximate the expected frequency of the clock signal (Fig. 2,

labels 200, 210), determines the length of the delay line corresponding to the period (Fig. 2, labels 200 and 210), and comparing the recovered clock signal with a data signal (Fig. 2, label 240, input data signal and recovered clock signal) and the recovered clock signal corresponds to the period of the reference clock signal (Fig. 2, label recovered clock signal, and local clock signal in delay line 210)

- h. **Claim 10**, Ozkan discloses a delay line corresponding to the period of the reference clock signal (Fig. 2, label 200 and 210), comparing (Fig. 2, label 270) a variable clock signal (Fig. 2, output from label 280 to 270) with a fixed clock signal (Fig. 2, local clock signal inputted into label 270) and the fixed clock signal having a constant phase relationship (Fig. 2, label 200) since the reference clock signal's, disclosed by Ozkan, does not change.
- i. **Claim 13**, Ozkan inherently discloses that the recovered signal is limited by the fixed position to the variable position since the counter (Fig. 2, label 230) outputs a selected signal depending on the input from the counter (Fig. 2, label 290), which selects the output from the first mux (Fig. 2, label 280) and the control signals (Fig. 2, output from label 240)
- j. **Claim 21**, Ozkan discloses a plurality of clock signals differing in phase (Fig. 2, label 210), a phase comparator for comparing a selected clock signal with a data signal to generate a change signal (Fig. 2, input data signal, label 240 and output from counter 230), a second selector for varying the selected clock signal based on the change signal (Fig. 2, output from counter 230) and range



signal (Fig. 2, output from counter 290), and a phase comparator (Fig. 2, label 270) for comparing a fixed clock signal (Fig. 2, local clock signal) with a variable clock signal (Fig. 2, output from mux 280 to label 270) to generate a range signal (output from counter 290).

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. **Claims 4, 14** are rejected under 35 U.S.C. 103(a) as being unpatentable over Ozkan (US Patent No.: 5488641) in view of Fawcett et al (US Patent No.: 6320436).
  - a. **Claim 4**, Fawcett et al discloses a reference clock signal (Fig. 2, label CLK1) delayed by delay elements, wherein the taps "can be delayed by a selected amount." (Col. 2, line 65-67 and Col. 3, line 1) It would be obvious to one skilled in the art to apply Fawcett et al's invention to the delay line disclosed by Ozkan to allow any amount of delay needed to synchronize the data signal with the reference clock signal.
  - b. **Claim 14** inherits the limitations of claim 4. Ozkan discloses a recovered clock signal is offset in frequency from the reference clock signal (Fig. 2, label 200),

since the recovered clock signal is delayed by a certain amount by the delay line. (Fig. 2, label 210 and recovered clock signal)

9. **Claim 20** is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakanishi et al (US Patent No.: 5579184) in view of Murata et al (US Patent No.: 5777567) and further in view of Ozkan (US Patent No.: 5488641).

a. **Claim 20**, Nakanishi et al discloses a digital phase locked loop comprising a phase comparator comparing the data signal and output signal and outputting a phase difference signal to a low pass filter and a reference digital phase locked loop comprised of a reference phase comparator comparing a fixed delayed signal and a reference signal and outputting a signal to the low pass filter.

Although Nakanishi et al does not disclose a digital phase locked loop comprising a delay element with selectable output, a selected signal outputted from the low pass filter and a reference digital phase locked loop comprising a delay element with a reference selectable output and the low pass filter forming a reference selector signal, Murata et al discloses a phase detector, low pass filter forming a selected signal to delay line and a reference selected signal to delay line. (Fig. 2, labels 210, 214, 216 and 204) It would be obvious to one skilled in the art to replace the function of the VCO disclosed by Nakanishi et al with the VCO, comprising a selectable delay line, disclosed by Murata et al to transfer low frequency signals to high frequency signals and accommodate data signals with high frequency. Although Nakanishi et al and Murata et al does not disclose a selector signal limited to a range set by a reference signal, Ozkan

inherently discloses the selector signal being limited to a range indicated by a reference signal. Based on Ozkan's description of the frequency relationship between the local clock signal (aka: reference signal) and input data signal, the dependency of the output of the counter (aka: selected signal) which is used to select the recovered clock signal (aka: output signal), Ozkan inherently discloses a selector signal limited by the reference clock signal and the data signal. (Col. 5, lines 26-40) It would be obvious to one skilled in the art to apply Ozkan's limitation to Nakanishi et al and Murata et al's invention to produce a delay line that would only contain the range of the reference signal to synchronize the data signal with the reference signal.

***Allowable Subject Matter***

10. **Claims 8, 11, 12, 15, 16, and 17** are would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.


Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linda Wong whose telephone number is 571-272-6044. The examiner can normally be reached on 9-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on (571) 272-3056. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LW



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